GENERAL INSTRUMENT

RA-3-9600

System RAM

FEATURES

- Memory area 352 words of 16 bits
- Address counter and control logic for D.M.A. operation
- Control decoder for CPU data control signals
- Memory map comparator and control logic for additional memory on 14 bit bus
- Current line buffer — 20 words of 14 bits
- Drive capability on 16 bit and 14 bit bus for 1 TTL load and 100pf

FUNCTIONAL DESCRIPTION

The RA-3-9600 is a dual port interface and 16 bit wide RAM storage area. The RA-3-9600 contains twenty 14 bit serial data buffer registers with separate bus control signals.

The RA-3-9600 memory is 352 x 16 bit contiguous words from address 512-863 with the graphics descriptors using the first 240 words. The graphics use only the lower 14 bits of each word leaving the two most significant bits available for user storage.

OPERATION DESCRIPTION

The RA-3-9600 RAM accepts data from the CPU via a 16 bit bi-directional bus which is time multiplexed with address and data. A 3 bit control bus from the CPU is used to provide strobe signals for the on-chip address latch and main memory area.

The RAM has two operating modes:
Mode 1 — On decoding an interrupt the RAM is enabled into a bus copy mode. In this mode the RAM copies the lower fourteen bits of the CPU bus onto the graphics bus. The direction of copy is always from the CPU and towards the graphics except during a bus reversal condition. The reversal condition is indicated when the CPU requests a read from an external graphics address on the 14 bit bus. Under this condition the 9600 will turn its 14 bit bus outputs into tri-state and gate the 14 bit bus through to the 16 bit CPU bus.

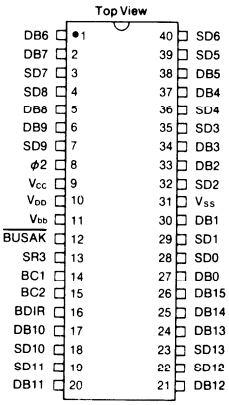
Mode 2—Is selected when the CPU issues $\overline{\text{BUSAK}}$ command (DMA request). The effect of $\overline{\text{BUSAK}}$ inside the 9600 is to reset the interrupt synchronizing logic and to switch the address decoder from the CPU address register to the graphics address counter. This counter, which sequences through the 240 words of graphics data, will have been previously set to zero when the interrupt signal was decoded. When the CPU is in the DMA state, the graphics system will prepare to display a new row of twenty characters and to load the 20 buffer registers within the 9600. For the first cycle of DMA after interrupt the graphics address counter will be at zero and the data at that address is passed to the 14 bit output. The action of SR3 will enable the output buffers and drive the 14 bit bus. The twenty shift registers are also loaded at this time. The negative edge of SR3 tri-states the 14 bit output and increments the graphics address counter. The shift registers are also clocked at this time. The SR3 input provides twenty positive pulses to the 9600 and loads the shift register buffers while giving the graphics the first row of characters. At the end of the first DMA cycle, after the CPU interrupt, the graphics address counter will be at value 20. The 9600 operation for the next fifteen lines will be to clock the 20 shift registers and gate the contents onto the 14 bit bus under control of the SR3 input. When the CPU is running and $\overline{\text{BUSAK}}$ is a logic 1, the graphics address counter is not incremented and it stays at the value 20. At the end of the first row of characters, the complete DMA operation is repeated and the address counter will be left at 40. This sequence occurs for the 12 rows of characters until all 240 have been successfully accessed.

The operation of SR3, INCREMENT/TRI-STATE signal, is to step the shift register sequentially through each of the twenty characters. If the $\overline{\text{BUSAK}}$ signal is low, i.e., in DMA, it also increments the graphics ADDRESS COUNTER. SR3 disables the 14 bit graphics bus during the low period.

At the end of active picture the STIC issues an interrupt request to the CPU. The RA-3-9600 tests for the INTAK* response from the CPU and uses this signal as an entry control for a copy mode between the two buses. The end of the copy mode is controlled by the first $\overline{\text{BUSAK}}$ negative edge.

*INTAK, equivalent BC1, BC2, BDIR = '1'

PIN CONFIGURATION
40 LEAD DUAL IN LINE



VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{BB} ..... −0.2V to +18.0V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} ..... −0.2V to +18.0V

Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C V_{CC} = +4.85V—+5.15V
V_{DD} = +11.6V—+12.4V V_{BB} = −3.3V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Clock Input Freq. $\phi 2$	—	—	—	—	MHz	1.79545MHz
Input Logic Low	V_{ILC}	0	—	0.7	Volts	
Input Logic High	V_{IHC}	2.4	—	V_{DD}	Volts	
Input Current	I_{ILC}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Inputs and Control Inputs						
Input Logic Low	V_{IL}	0	—	0.7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Currents	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{IL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OL}	2.4	—	V_{CC}	Volts	+100pF
AC CHARACTERISTICS						
Clock Input					ns	
Rise & Fall Time	t_r, t_f	—	—	50	ns	
CPU Bus Timing						
Address Set Up Time	t_{as}	300	—	—	ns	
Address Hold Time	t_{ao}	—	—	50	ns	
Data Access Time	t_{da}	—	—	500	ns	1 TTL Load
Data Hold Time	t_{do}	—	100	—	ns	+100pF
Write Data Setup	t_{ws}	100	—	—	ns	
Write Data Hold	t_{as}	0	—	—	ns	
Graphics Bus Timing						
Data Access Time	t_{ga}	—	—	150	ns	1 TTL Load
Data Hold Time	t_{go}	—	100	—	ns	+100pF

VIDEO

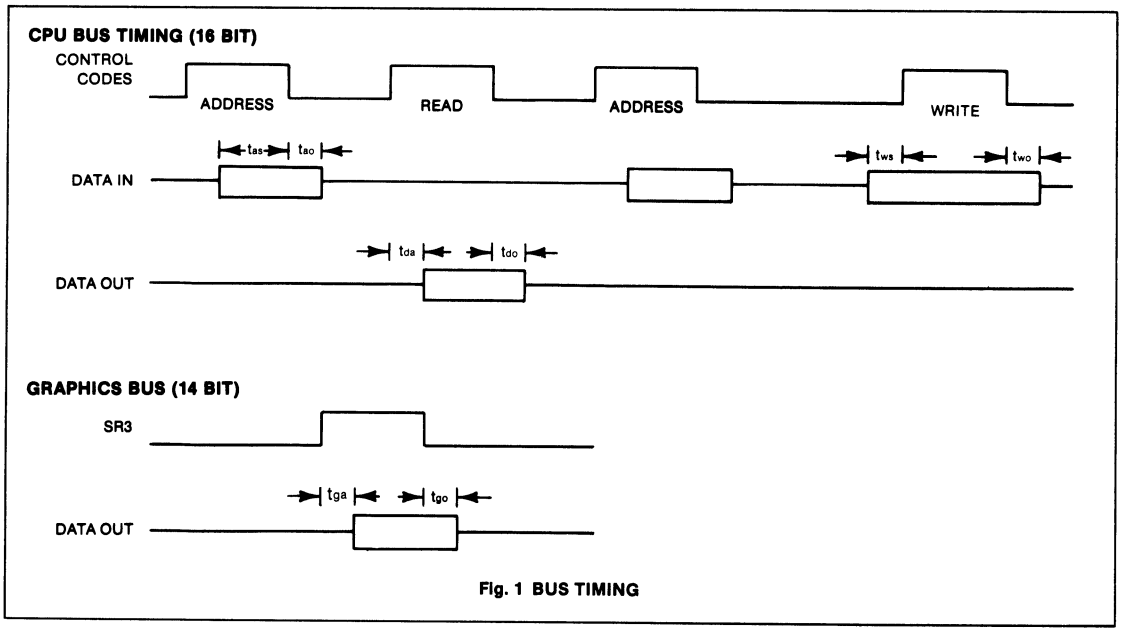


Fig. 1 BUS TIMING

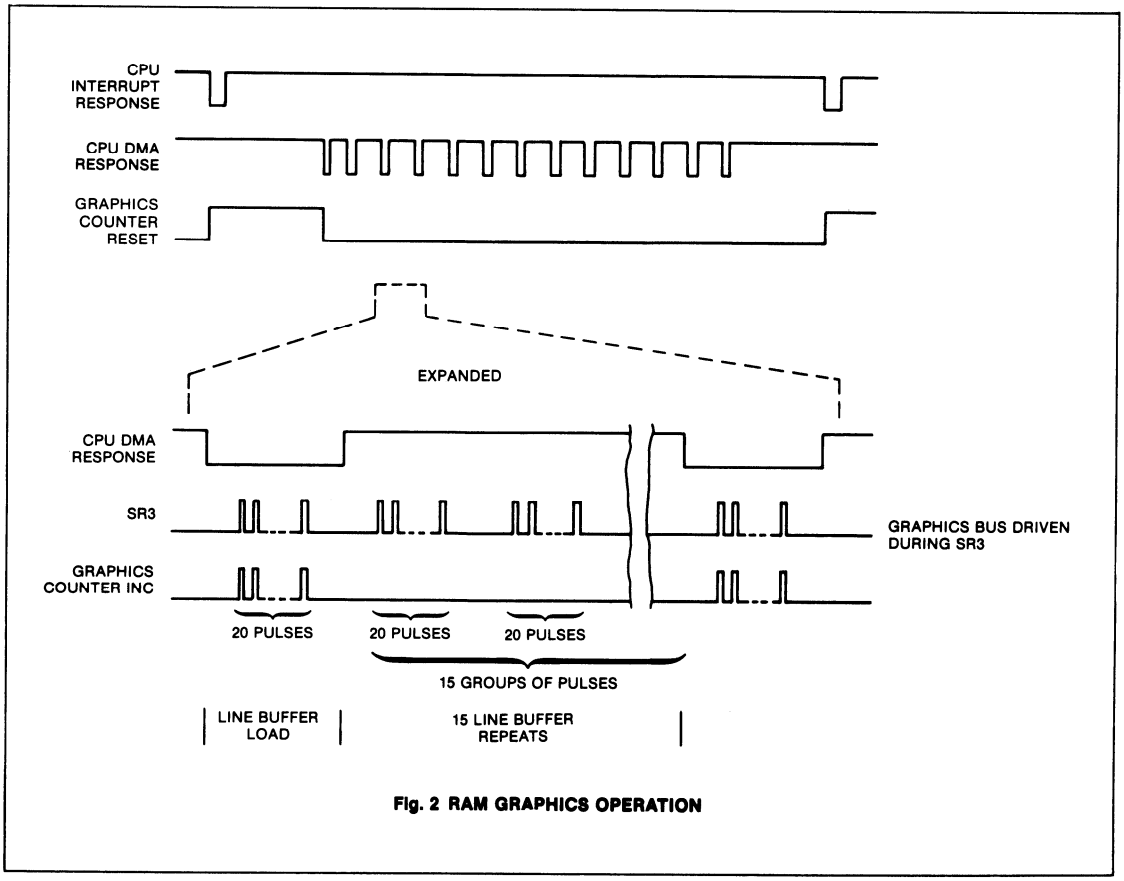


Fig. 2 RAM GRAPHICS OPERATION